ABSTRACT

Systems and methods of processing addresses provide for receiving a full linear address of an instruction and reducing a size of the full linear address to obtain a reduced linear address. A data block can be retrieved from a data array if the reduced linear address corresponds to a tag in a tag array, where the tag array is associated with the data array. The reduced linear address enables the tag array to either be smaller in size or achieve enhanced performance. The data array may be a prediction array of a branch predictor or a cache array of a cache.